In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the mandatory amendment format.

1. (Currently Amended) A method of translating instructions, said method comprising:

translating a first block of instructions executable in a first processor architecture**[[,]]** into a translated first block of instructions executable in a second processor architecture, said translated first block of instructions operating with a stack of data entry positions; **[[**and**]]**

during the translating, generating an expected Top of Stack (TOS) position in said stack for said first block of instructions; and

during the translating, adding at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS position in said stack at a time of executing said translated first block of instructions;

wherein said at least one instruction branches to correction code if said expected TOS is not equal to said actual TOS, ~~and wherein~~ said correction code to generate a delta of said expected TOS and said actual TOS and to adjust said stack for said first block of instructions by the delta at the time of executing said translated first block of instructions.

2.-3. (Canceled)

4. (Previously Presented) The method as claimed in claim 1, said method further comprising:

determining if execution of instructions in said first block of instructions changes the actual TOS.

5. (Previously Presented) The method as claimed in claim 4, said method further comprising:

in response to determining execution of instructions in said first block of instructions changes the actual TOS, adding an instruction to an end of the first block of instructions to update the actual TOS.

6. (Currently Amended) A computer-readable medium having stored thereon a set of instructions to translate instructions, said set of instructions, which when executed by a processor, cause said processor to perform a method comprising:

translating a first block of instructions executable in a first processor architecture**[[,]]** into a translated first block of instructions executable in a second processor architecture, said translated first block of instructions operating with a stack of data entry positions;

during the translating, generating an expected Top of Stack (TOS) position in said stack for said first block of instructions; and

during the translating, adding at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS at a time of executing said translated first block of instructions;

wherein said at least one instruction branches to correction code if said expected TOS is not equal to said actual TOS, ~~and wherein~~ said correction code to generate a delta of said expected TOS and said actual TOS and to adjust said stack for said first block of instructions by the delta at the time of executing said translated first block of instructions.

7.-8. (Canceled)

9. (Previously Presented) The computer-readable medium as claimed in claim 6, wherein said set of instructions further includes additional instructions, which when executed by said processor, cause said processor to perform said method further comprising:

determining if execution of instructions in said first block of instructions changes the actual TOS.

10. (Previously Presented) The computer-readable medium as claimed in claim 9, wherein said set of instructions further includes additional instructions, which when executed by said processor, cause said processor to perform said method further comprising:

in response to determining execution of instructions in said first block of instructions changes the actual TOS, adding an instruction to an end of the first block of instructions to update the actual TOS.

11. (Currently Amended) A system comprising:

a first unit of logic to translate a first block of instructions executable in a first processor architecture[[,]] into a translated first block of instructions executable in a second processor architecture, said translated first block of instructions operating with a stack of data entry positions; and

a second unit of logic to generate an expected Top of Stack (TOS) position in said stack for said first block of instructions, wherein said second unit of logic further adds at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS at a time of executing said translated first block of instructions;

wherein said at least one instruction branches to correction code if said expected TOS is not equal to said actual TOS, ~~and wherein~~ said correction code to generate a delta of said

expected TOS and said actual TOS and to adjust said stack for said first block of instructions by the delta at the time of executing said translated first block of instructions.

12.-13. (Canceled)

14. (Previously Presented) The system as claimed in claim 11, wherein said second unit of logic determines if execution of instructions in said first block of instructions changes the actual TOS.

15. (Previously Presented) The system as claimed in claim 14, wherein said second unit of logic, in response to determining execution of instructions in said first block of instructions changes the actual TOS, adds an instruction to an end of the first block of instructions to update the actual TOS.

16. (Previously Presented) The method as claimed in claim 1, wherein to adjust said stack for said first block of code by the delta includes rotating said stack by the delta.

17. (Previously Presented) The computer-readable medium as claimed in claim 6, wherein to adjust said stack for said first block of code by the delta includes rotating said stack by the delta.

18. (Previously Presented) The system as claimed in claim 11, wherein to adjust said stack for said first block of code by the delta includes rotating said stack by the delta.

19. (Previously Presented) The method as claimed in claim 5, wherein to update the actual TOS results in an expected TOS corresponding to a second block of instructions

matching the actual TOS, said second block of instructions following said first block of instructions in execution and further operating with said stack.

20. (Previously Presented) The computer-readable medium as claimed in claim 10, wherein to update the actual TOS results in an expected TOS corresponding to a second block of instructions matching the actual TOS, said second block of instructions following said first block of instructions in execution and further operating with said stack.

21. (Previously Presented) The system as claimed in claim 15, wherein to update the actual TOS results in an expected TOS corresponding to a second block of instructions matching the actual TOS, said second block of instructions following said first block of instructions in execution and further operating with said stack.